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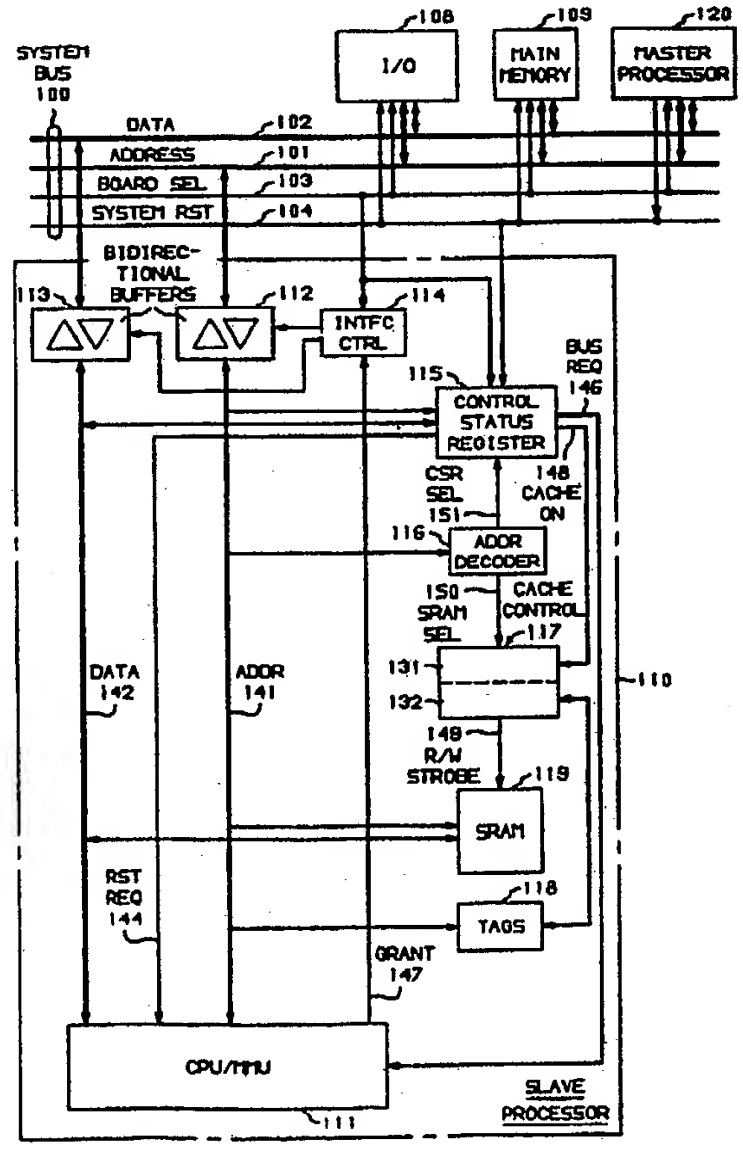
(57) Abstract

In a master-slave multiprocessor, a slave processor (110) includes a random access memory array (119) that serves at initialization time as the slave processor's boot memory and that serves during normal operation time as the slave processor's cache memory. A master processor (120) writes the slave processor's boot program into the memory array when the memory array is to serve as the boot memory, i.e., following system reset.



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MULTI-PURPOSE MEMORY

Technical Field

The invention relates to processors in general and to memories of data processors in particular.

Background of the Invention

Today's typical processor includes special purpose memories provided to enhance ease of use and performance of the processor. Included among these memories are a boot memory--typically a read only memory (ROM)--that stores a boot program whose execution by the processor's central processing unit (CPU) upon system power-up or reset automatically initializes the CPU, and a cache memory--implemented as a random access memory (RAM)--that serves during normal processor operation as a high-speed buffer for information--illustratively either or both data and instructions--passing between the CPU and the processor's main on-line memory.

Storage devices used to implement such memories add to the cost of the processor, and also occupy valuable circuit board space. The latter is especially a serious consideration in the case of single-board processors, where a whole processor is implemented on a single circuit board. In such processors, providing of such special-purpose memories may potentially be done only at the sacrifice of some other processor capabilities, because circuit board space may not be available for circuitry needed to implement both.

Accordingly, it is a problem in the prior art to provide special-purpose memory functions in a processor with the minimum number of memory devices so as to minimize processor cost and to occupy minimum circuit board space.

Summary of the Invention

The invention is directed to solving these and other problems of the prior art. According to the invention, there is provided a memory that serves as different special-purpose memories at different times. A control arrangement causes the memory at one time to serve a first function exclusive of a second function, and at another time to serve the second function exclusive of the first function. Specifically, an apparatus such as a processor includes a processing unit, a memory coupled to the processing unit, and an arrangement coupled to the memory for selectively causing the memory: (a) to store at one time a boot program for execution by the processing unit at initialization, and (b) to buffer at another time information passing between the processing unit and another memory during normal operation. The memory is thus caused to selectively serve as either a boot memory or a cache memory for the processing unit. The apparatus further includes means for effecting storage of the boot program in the memory when the memory is serving as the boot memory. Illustratively, the apparatus is a multiprocessor wherein the processing unit and memory are parts of one processor and the means for effecting storage of the boot program in the memory is another processor.

Because the memory serves different functions at different times, separate memory devices need not be included in the system to implement each function. Rather, the functions are all implemented via the same memory device. Elimination of extra memory devices beneficially lowers system cost and reduces the circuit board area occupied by memory devices.

These and other advantages and features of the present invention will become apparent from the following description of an illustrative embodiment of the invention taken together with the drawing.

Brief Description of the Drawing

FIG. 1 is a block diagram of a processing system that includes an illustrative embodiment of the invention; and

FIG. 2 flowcharts relevant portions of initializing operations of the master processor of FIG. 1.

Detailed Description

FIG. 1 shows a multiprocessor system. Illustratively, this system is the 3B2/600 computer of AT&T expanded into a master-slave multiprocessor configuration by connection thereto of a second processor. The original processor of the 3B2/600 computer functions as master processor 120 of the system. The added second processor functions as slave processor 110. Illustratively, processor 110 is substantially a duplicate of processor 120, modified as described below. Slave processor 110 is connected to an input and output (I/O) slot of system bus 100 of the 3B2/600 computer. Illustratively, a main on-line memory 109 and an I/O subsystem 108 such as a disk are connected to other slots of system bus 100. Bus 100 connects units 108-110 to master processor 120 for communication.

System bus 100 includes an ADDRESS bus 101, a DATA bus 102, BOARD SELECT lines 103, and a SYSTEM RESET line 104.

Slave processor 110 includes a central processing unit (CPU) and memory management unit (MMU) 111. Illustratively, CPU/MMU 111 comprises the WE 32100 microprocessor chip set. CPU/MMU 111 is connected to ADDRESS bus 101 and DATA bus 102 through bidirectional tri-state buffers 112 and 113, respectively. DATA lines 142 connect CPU/MMU 111 to buffer 113 while ADDRESS lines 141 connect CPU/MMU 111 to buffer 112. Buffers 112 and 113 are under control of interface controller 114, which is connected to the one of the BOARD SELECT lines 103 that is associated with slave processor 110, and to CPU/MMU 111 via a GRANT line 147.

Slave processor 110 also includes a control status register (CSR) 115. CSR 115 is connected to the one line of BOARD SELECT lines 103 that is associated with slave processor 110, and, in addition, is connected to SYSTEM RESET line 104, DATA lines 142, ADDRESS lines 141, a RESET REQUEST line 144, a BUS REQUEST line 146, and a CACHEON line 148. Lines 144 and 146 connect CSR 115 with CPU/MMU 111.

Slave processor 110 further includes a static random access memory (SRAM) array 119. SRAM array 119 is connected to ADDRESS lines 141 and DATA lines 142. SRAM array 119 is controlled by a cache controller 117 through a read and write (RW) strobe line 149.

As the name implies, cache controller 117 typically causes SRAM array 119 to function as a cache memory. Logically, cache controller 117 is divided into two control portions 131 and 132, each of which is active at different times and each of which causes SRAM array 119 to operate in a different mode. Control portion 132 causes array 119 to operate in conventional cache memory mode, as a virtual address-and-data cache memory for buffering information passing between CPU/MMU 111 and main memory 109. Control portion 132 is aided by a conventional tag memory 118 associated with array 119 and communicatively connected to control portion 132. Tag memory 118 is also connected to ADDRESS lines 141. Control portion 131 causes array 119 to operate in "diagnostic" mode, wherein individual locations of array 119 may be addressed and read or written. Control portion 131 is aided by a conventional address decoder 116. Decoder 116 is connected to control portion 131 by SRAM SELECT line 150, is connected to CSR 115 by CSR SELECT line 151, and is also connected to ADDRESS lines 141. Selection of which one of the two control portions 131 and 132 is active and in control of array 119, and hence in which mode array 119 is operating, is made by CSR 115 via a CACHEON line 148.

Operational aspects of the system of the FIG. 1 that are relevant to an understanding of the invention will now be described in conjunction with FIG. 2.

Upon system power-up or re-initialization, master processor 120 pulses (momentarily asserts) SYSTEM RESET line 104, at step 200. This action sets a RESET bit and a HALT bit of CSR 115. Setting of the HALT bit leads CSR 115 to assert BUS REQUEST line 146. Setting of the RESET bit leads CSR 115 to assert RESET REQUEST line 144.

CPU/MMU 111 responds to assertion of RESET REQUEST line 144 by resetting slave processor 110, including clearing certain bits in CSR 115, in particular the RESET bit and a CACHEON bit. Clearing of the RESET bit and the CACHEON bit causes CSR 115 to deassert RESET REQUEST line 146 and CACHEON line 148. CPU/MMU 111 responds to the request signal on BUS REQUEST line 146, which indicates the highest priority request for access to ADDRESS and DATA lines 141 and 142, by asserting GRANT line 147 and by stopping further activities. CPU/MMU 111 then waits for BUS REQUEST line 144 to be deasserted.

Following its momentary assertion of SYSTEM RESET line 104, master processor 120 retrieves a boot program for initializing CPU/MMU 111 from either main memory 109 or secondary memory--disk--of I/O subsystem 108, at step 201, and effects storage of the program in SRAM 119, at step 202. Illustratively, it does so as follows.

After it has retrieved an instruction of the boot program from memory, master processor 120 asserts the line of the BOARD SELECT lines 103 that is associated with slave processor 110, places an address of the address spectrum of SRAM array 119 at which the instruction is to be stored on ADDRESS bus 101, and places the instruction on DATA bus 102.

Assertion of slave processor's BOARD SELECT line 103 while GRANT line 147 is asserted causes interface control 114 to open buffers 112 and 113 thereby to

transfer the information from ADDRESS and DATA buses 101 and 102 onto ADDRESS and DATA lines 141 and 142, respectively. Address decoder 116 examines the address appearing on ADDRESS lines 141. When it detects an address lying within the address spectrum of SRAM array 119, it asserts SRAM SELECT line 150.

Cache control portion 131 responds to signals on SRAM SELECT line 150 while CACHEON line 148 is deasserted, by issuing a strobe signal to SRAM array 119 via R/W strobe line 149. SRAM array 119 responds to the strobe signal by storing the instruction conveyed by DATA lines 142 in the location addressed by ADDRESS lines 141.

This process is repeated until master processor 120 has stored the whole boot program in SRAM array 119. Master processor 120 then accesses and writes CSR 115 to reset the HALT bit, at step 203, in the same manner as it writes SRAM array 119. Address decoder 116 recognizes the address generated by master processor 120 as being an address of CSR 115. Address decoder 116 therefore asserts CSR SELECT line 151 to cause CSR 115 to respond to the address and data appearing on ADDRESS lines 141 and DATA lines 142, respectively. The response of CSR 115 thereto is to reset its HALT bit and, consequently, to deassert BUS REQUEST line 146.

Deassertion of BUS REQUEST line 146 causes CPU/MMU 111 to continue its normal operation. Following reset, this operation involves initialization, which begins by execution of a boot program stored beginning at a predetermined address in memory. This address is set to be the SRAM array 119 address at which the boot program begins. Accordingly, CPU/MMU 111 generates an SRAM array 119 address on ADDRESS lines 141. This address is recognized as an SRAM array 119 address by address decoder 116, which responds by asserting SRAM SELECT line 150. CACHEON line 148 is still deasserted, so cache control portion 131 is active, and it responds to assertion of SRAM SELECT line 150 by issuing a strobe to

SRAM array 119 on R/W strobe line 149. SRAM array 119 responds to the strobe signal by outputting on DATA lines 142 the instruction stored at the address appearing on ADDRESS lines 141. CPU/MMU 111 then receives the instruction over DATA lines 142 and executes it. This cycle is repeated until CPU/MMU 111 completes execution of the boot program. Hence, SRAM array 119 serves as the boot memory for CPU/MMU 111.

Having been booted, CPU/MMU 111 can now begin to access and execute programs from main memory 109. These may be further initialization programs, for example. Upon completion of initialization, when CPU/MMU 111 is about to enter normal operating mode including virtual addressing mode, CPU/MMU 111 sets the CACHEON bit of CSR 115. CPU/MMU 111 accesses the CSR 115 by generating the address of CSR 115 on ADDRESS lines 141. The address is recognized by address decoder 116, which asserts CSR SELECT line 151 in response. CSR 115 responds to assertion of CSR SELECT line 151 by allowing CPU/MMU 111 a write access to CSR 115 via the ADDRESS and DATA lines 141 and 142.

CSR 115 responds to setting of the CACHEON bit by asserting CACHEON line 148. Assertion of CACHEON line 148 disables cache control portion 131, so that it no longer responds to assertions by address decoder 116 of SRAM SELECT line 150, and enables cache control portion 132 to control SRAM 119. As was mentioned above, control portion 132 causes SRAM 119 to function as a virtual data-and-instruction cache memory for CPU/MMU 111, in a conventional manner. Upon being enabled, control portion 132 initializes the cache by flushing, that is, invalidating, its contents.

Henceforth, the system of FIG. 1 functions conventionally, until the next time that system reset line 104 is asserted. At that time, the operations described herein are repeated.

Of course, various changes and modifications to the illustrative embodiment described above will be apparent to those skilled in the art. For example, the system of FIG. 1 may include more than one slave processor 110. Or, the system may be a uniprocessor, wherein the multi-purpose memory of the single processor is loaded with the boot program by some other system unit, such as an I/O controller. Also, other functions, such as scratch memory functions, may be included among the functions of the multi-purpose memory. Such changes and modifications can be made without departing from the spirit and the scope of the invention and without diminishing its attendant advantages. It is therefore intended that such changes and modifications be covered by the following claims.

Claims

1. An apparatus (FIG. 1) including a memory (119) and equipment coupled to the memory, characterized in that the equipment includes:

means (115-118, 120) for causing the memory at one time to serve a first function exclusive of a second function, and for causing the memory at another time to serve the second function exclusive of the first function.

2. The apparatus of claim 1 wherein the equipment includes a processor (111) and a second memory (109) coupled to the processor, characterized in that the means comprise

means (115-118, 120) for causing the one memory at one time to store an initialization program for execution by the processor, and at another time to buffer information passing between the processor and the second memory.

3. The apparatus of claim 1 wherein the equipment includes a processor (111), characterized in that the means comprise

means (115-118) for selectively causing the memory to serve as one of (a) a boot memory for the processor and (b) a cache memory for the processor; and

means (120) for effecting storage in the memory of a boot program for the processor when the memory is serving as a boot memory.

4. The apparatus of claim 1 wherein the equipment includes a processor (111), characterized in that the means comprise

means (115-118, 120) for causing the memory at one time to serve as a boot memory for the processor and at another time to serve as a cache memory for the processor.

5. The apparatus of claim 4 characterized in that the means include

means (120) for effecting storage in the memory of a boot program for the processor when the memory is serving as a boot memory.

6. The apparatus of claim 4 characterized in that the means include

first means (116, 131) coupled to the memory, when activated for causing the memory to function as a boot memory for the processor,

second means (113, 132) coupled to the memory, when activated for causing the memory to function as a cache memory for the processor, and

third means (115) connected to the first and the second means, for selectively activating one of the first and the second means while deactivating the other of the first and the second means.

7. The apparatus of claim 6 wherein the causing means further include

a second processor (120) for causing the third means to activate the first means and for effecting storage in the memory of a boot program for the processor while the first means are activated.

8. A method of operating a memory (119), characterized by the steps of:

activating a first memory control means (131) and deactivating a second memory control means (132), in response to receipt of a first signal;

operating the memory in a first mode of operation under control of the active first memory control means, wherein the memory serves a first function exclusive of a second function;

deactivating the first memory control means and activating the second memory control means, in response to receipt of a second signal; and

operating the memory in a second mode of operation under control of the active second memory control means, wherein the memory serves the second function exclusive of the first function.

9. The method of claim 8 characterized in that

the memory functions as a boot memory in the first mode of operation; and

the memory functions as a cache memory in the second mode of operation.

10. The method of claim 9 characterized in that the step of operating the memory in the first mode of operation comprises the step of:

storing (FIG. 2) a boot program in the memory.

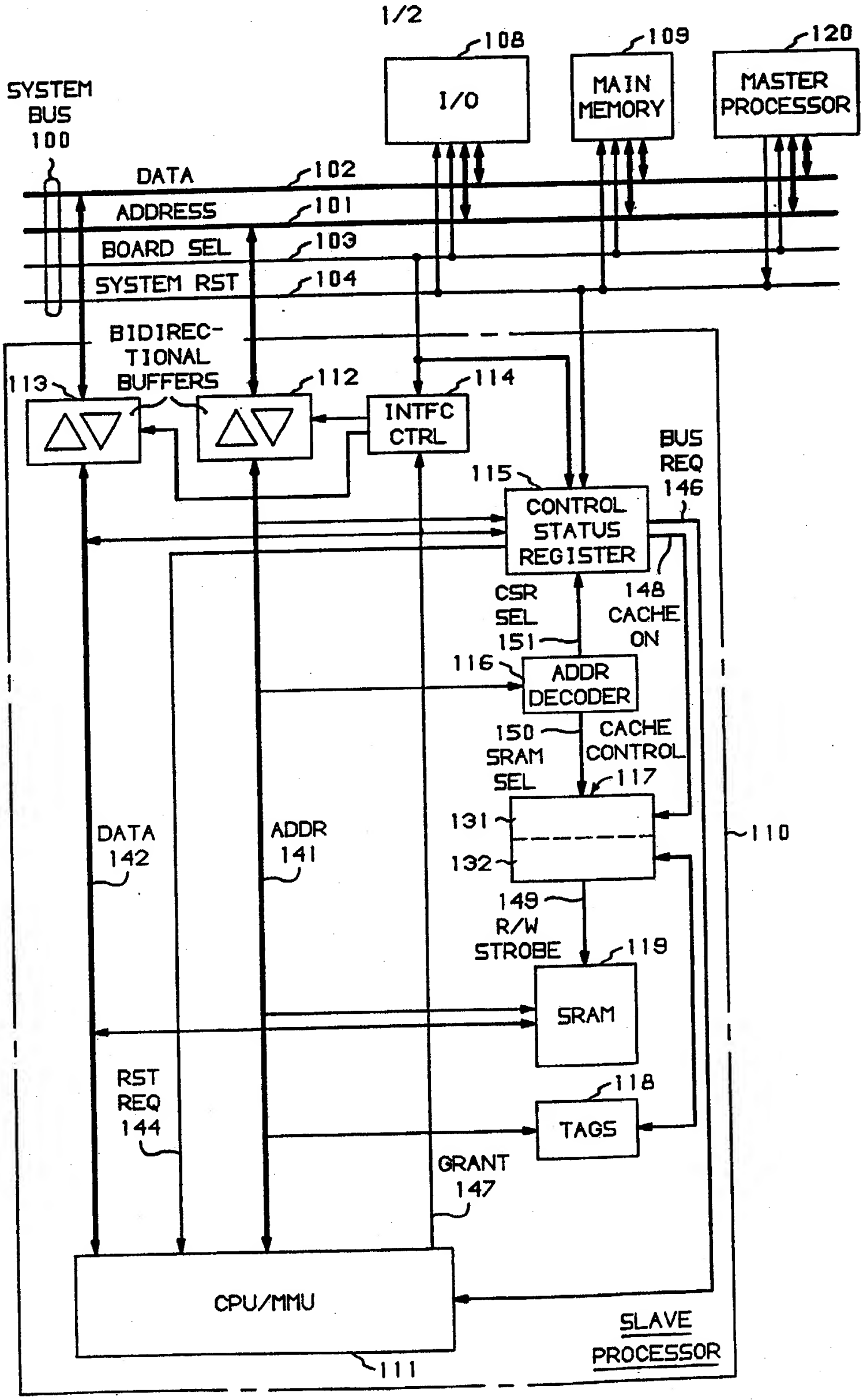
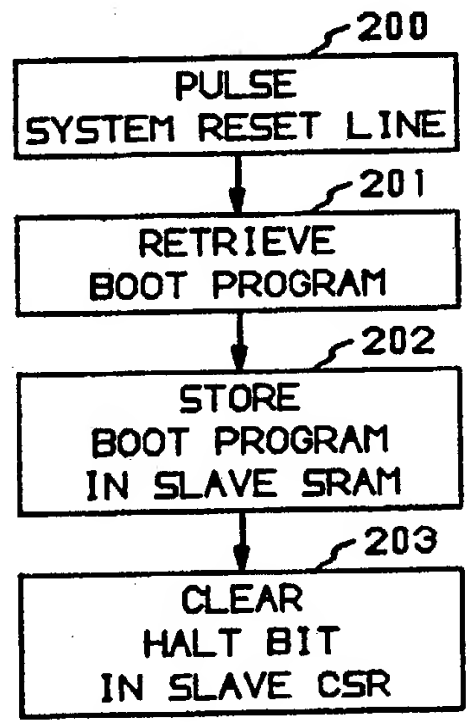

SYSTEM BUS 100
I/O
108
MAIN MEMORY
109
MASTER PROCESSOR
120
DATA
102
ADDRESS
101
BOARD SEL
103
SYSTEM RST
104
BIDIREC-TIONAL BUFFERS
113
112
INTFC CTRL
114
BUS REQ 146
115
CONTROL STATUS REGISTER
CSR SEL 151
148 CACHE ON
116
ADDR DECODER
150 SRAM SEL
CACHE CONTROL
117
131
132
110
DATA 142
ADDR 141
149 R/W STROBE
119
SRAM
RST REQ 144
118
TAGS
GRANT 147
CPU/MMU
111
SLAVE PROCESSOR

FIG. 1

FIG. 2


200
PULSE
SYSTEM RESET LINE
201
RETRIEVE
BOOT PROGRAM
202
STORE
BOOT PROGRAM
IN SLAVE SRAM
203
CLEAR
HALT BIT
IN SLAVE CSR

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 87/02155

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: G 06 F 9/44; G 06 F 12/08

II. FIELDS SEARCHED

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Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X	IBM Techical Disclosure Bulletin, volume 21, no. 10, March 1979, (New York, US), R.J. Gallagher: "Read-only storage/ random-access memory mode change", pages 4100-4101 see the whole document	1,8
A	--	2-6,9,10
A	IBM Techical Disclosure Bulletin, volume 20, no. 10, March 1978, (New York, US), S.G. Hogan et al.: "Loading and running a program without main storage", page 4032 see the whole document	1-6,8-10
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* Special categories of cited documents: [10]

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IV. CERTIFICATION

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